Goa Vidyaprasarak Mandal's
Gopal Govind Poy Raiturcar College of Commerce and Economics
Farmagudi, Ponda-Goa.

B.C.A. (Semester - I) Examination – October 2014

COMPUTER ORGANIZATION AND ARCHITECTURE

Duration : 2 hours **Marks : 50**

Instructions **:** ***A.) All the questions are compulsory.***
B.) Draw neat diagrams with pencil wherever required.

I. 1. State whether the following statements are True or False. (1mk x 5 = 5 mks)

a) CISC systems does not shorten execution time by reducing the number of instructions per program.

b) Each micro-instruction specifies single or few micro-operations to be performed is called vertical microprogramming.

c) A sequence of instructions is known as a micro-program or firmware.

d) The control bus portion of the system bus provides signals to the control unit.

e) Execution unit does not remove instructions from the instruction queue.

2. Answer the following. (1mk x 5 = 5 mks)

a) What is Magnetic Tape ?

b) What is Data Buffering ?

c) What are the elements of an Instruction ?

d) What are the types of Operand ?

e) What is the meaning of the following instruction ?

MOV AH, 01

II. 1. Explain the Direct Addressing with an example. (2 mks)

2. Explain the operation of DRAM. (3 mks)

3. Explain the major computer operations and draw the block diagram of the computer. (5 mks)

III. 1. Perform the following operations. (1 mk x 2 = 2 mks)

i. (+3) + (+4)

ii. (–4) + (+4)

2. Perform the following conversions. (1.5 mk x 2 = 3 mks)

i. $(11001)_2 = (X)_{10}$

ii. $(32)_{10} = (X)_2$

3. Explain the Single bus, Integrated DMA-I/O configuration with the diagram. (5 mks)

IV. 1. Explain the Program Status Word. (2 mks)

2. Explain the InfiniBand Architecture. (3 mks)

3. Explain the Three-Level cache organization with the diagram. (5 mks)

V. 1. Explain the Fetch Cycle and the Execute Cycle. (2 mks)

2. Explain the 8086 Instruction sets with the appropriate examples. (3 mks)

3. Explain the general model of the Control Unit with the block diagram. (5 mks)

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