Goa Vidyaprasarak Mandal's

Gopal Govind Poy Raiturcar College of Commerce and Economics

Ponda-Goa

B.C.A. (Semester - I) Supplementary Examination – May/June 2019

COMPUTER ORGANIZATION AND ARCHITECTURE

Duration : 2 hours **Marks : 50**

Instructions : *A.) All the questions are compulsory.*
B.) Draw neat diagrams with pencil wherever required.

I. 1. State whether the following statements are True or False. (1mk x 5 = 5 mks)

a) CISC stands for Complex Instruction Set Computer.
b) In Direct Addressing, address field contains address of operand.
c) Interrupt driven and Programmed I/O require active CPU intervention.
d) In machine code each instruction does not have a unique bit pattern.
e) Bus Interface Unit does not contain the Instruction queue.

2. Answer the following. (1mk x 5 = 5 mks)

a) What is Semiconductor Memory ?
b) What are the types of Operand ?
c) What is Immediate Addressing ?
d) What is Loop Buffer ?
e) What is Assembly Language ?

II. 1. Explain the Fetch Cycle and the Execute Cycle. (2 mks)
2. Explain the 8086 Instruction Sets with appropriate examples. (3 mks)
3. Explain the Traditional Bus Architecture with the diagram. (5 mks)

III. 1. Perform the following operations. (1 mk x 2 = 2 mks)

i. (+3) + (+4)
ii. (–7) + (+5)

2. Perform the following conversions. (1.5 mk x 2 = 3 mks)

i. $(85)_{10} = (X)_2$
ii. $(11001)_2 = (X)_{10}$

3. Explain the Three-Level cache organization with the diagram. (5 mks)

IV. 1. Explain the difference between RAID 3 and RAID 4. (2 mks)
2. Explain the Vertical Micro-programming. (3 mks)
3. Explain the model of Control Unit with the diagram. (5 mks)

V. 1. Explain the structure of the Dynamic RAM. (2 mks)
2. Explain the functions of I/O Module. (3 mks)
3. Explain the DMA Module with the diagram. (5 mks)

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